WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein one or more wiring trenches are formed in each of said plurality of wiring insulating films along a periphery of said semiconductor chip in such a manner as to surround said circuit formation portion,

wherein in each of said one or more wiring trenches, a conductive layer made up of copper or a copper-based conductive material is buried via a first copper diffusion preventing film, in such a manner that the respective wiring trenches corresponding to each other in said plurality of wiring insulating films are connected with each other upwardly or downwardly, and

wherein a second copper diffusion preventing film is formed between each of said plurality of wiring insulating films and an other one of said plurality of wiring insulating films being adjacent thereto upwardly or downwardly, in such a manner as to be connected with the corresponding first copper diffusion preventing film.

2. The semiconductor device according to claim 1, wherein said at least one conductive layer is connected to a diffusion region formed in said semiconductor substrate.

3. The semiconductor device according to claim 1, wherein at least one of said plurality of wiring insulating films comprises a low-dielectric constant film.

4. A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein at least one seal ring made of a conductive material is formed along a periphery of said semiconductor chip so as to surround said circuit formation portion, said at least one seal ring being connected with said semiconductor substrate and being buried in said plurality of wiring insulating films in such a manner as to extend over said wiring insulating films.

5. A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein a plurality of seal rings each made of a conductive material is formed along a periphery of said semiconductor chip so as to surround said circuit formation portion, said seal ring beings connected with said semiconductor substrate and being buried in said plurality of wiring insulating films in such a manner as to extend over said wiring insulating films, and

wherein one or more slit-like notches are formed at specified positions in said plurality of seal rings in such a manner that the respective slit-like notches in two seal rings being adjacent to each other are not aligned.

6. The semiconductor device according to claim 4, wherein, said at least one seal ring comprises a damascene wiring structure as well as said multi-layer interconnection of said circuit formation portion.

7. The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a single damascene wiring structure.

8. The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a dual damascene wiring structure.

9. The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a combination of a single damascene wiring structure and a dual damascene wiring structure.

10. The semiconductor device according to claim 4, wherein said at least one seal ring is connected to a diffusion region formed in said semiconductor substrate.

11. The semiconductor device according to claim 4, wherein said at least one seal ring is connected via a contact to a

diffusion region formed in said semiconductor substrate, said contact and said diffusion region being formed so as to match approximately said at least one seal ring in shape.

12. The semiconductor device according to claim 4, wherein said at least one seal ring is connected via a contact to a diffusion region formed in said semiconductor substrate, said contact and said diffusion region being formed without matching said at least one seal ring.

13. The semiconductor device according to claim 4, wherein said at least one seal ring comprises copper or a copper-based conductive material.

14. The semiconductor device according to claim 4, wherein at least one of said plurality of wiring insulating films comprises a low-dielectric constant film.

15. A method for manufacturing a semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films, said method comprising:

a first step for forming a diffusion region on said semiconductor substrate and then forming a first wiring insulating film on said semiconductor substrate to form a plurality of first wirings in said first wiring insulating film

so as to surround said circuit formation portion and be connected respectively with said diffusion region;

a second step for forming a second wiring insulating film on said plurality of first wirings and said first wiring insulating film, and then forming a plurality of via wirings in said second wiring insulating film so as to surround said circuit formation portion and be connected respectively with the corresponding first wiring; and

a third step for forming a third wiring insulating film on said via wirings and said second wiring insulating film, and then forming a plurality of second wirings in said third wiring insulating film so as to surround said circuit formation portion and be connected respectively with the corresponding via wiring.

16. The method for manufacturing a semiconductor device according to claim 15, wherein said second step and said third step are repeated alternately, hereby forming sequentially a third insulating film wherein a plurality of third wirings is buried, and a subsequent insulating film wherein a plurality of subsequent wirings is buried.

17. The semiconductor device manufacturing method according to claim 15, wherein when forming said plurality of first wiring, said plurality of via wirings and said plurality of second wirings to form a plurality of seal rings, one or more slit-like notches are formed at specified positions on each of the plurality of seal rings.

18. A method for manufacturing a semiconductor device

comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films, the method comprising:

a first step for forming a diffusion region on said semiconductor substrate and then forming a first wiring insulating film on said semiconductor substrate to form a plurality of first wirings in said first wiring insulating film so as to surround said circuit formation portion and be connected respectively with said diffusion region; and

a second step for forming a second wiring insulating film on said plurality of first wirings and said first wiring insulating film and forming sequentially a third wiring insulating film on said second wiring insulating film, and then forming simultaneously a plurality of via wirings in said second wiring insulating film and a plurality of second wirings in said third wiring insulating film, so as to surround said circuit formation portion and be respectively connected with the corresponding first wiring.

19. The method for manufacturing a semiconductor device according to claim 18, wherein said second step is repeated, hereby forming sequentially a third insulating film wherein a plurality of third wirings is buried, and a subsequent insulating film wherein a plurality of subsequent wirings is buried.

20. The semiconductor device manufacturing method

according to claim 18, wherein said second step, after said second wiring insulating film and said third wiring insulating film are formed sequentially on said plurality of first wirings and said first wiring insulating film, comprises a step of forming simultaneously a plurality of wiring trenches in said third wiring insulating film and a plurality of via wiring trenches in said second wiring insulating film, a plurality of wiring trenches each communicate with the corresponding via wiring trench.

21. The semiconductor device manufacturing method according to claim 18, wherein when forming said plurality of first wirings, said plurality of via wirings and said plurality of second wirings to form a plurality of seal rings, one or more slit-like notches are formed at specified positions on each of the plurality of seal rings.

22. A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein an assembly pad, a characteristics evaluation pad, or a screening evaluation pad each are formed on a surface of said semiconductor substrate in such a manner to be electrically connected to said circuit formation portion, and

wherein at least one seal ring made of a conductive material is formed in such a manner as to surround said assembly pad, said characteristics evaluation pad, or said screening evaluation pad,

said at least one seal ring being connected with said semiconductor substrate and extending over said wiring insulating films.

23. The semiconductor device according to claim 22, wherein, at least one bottomed seal ring, being not connected with said semiconductor substrate, is formed in such a manner as to surround said assembly pad, said characteristics evaluation pad, or said screening evaluation pad.

24. The semiconductor device according to claim 22, wherein said at least one seal ring comprises a damascene wiring structure.

25. The semiconductor device according to claim 23, wherein said at least one bottomed seal ring comprising a damascene wiring structure.

26. A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein a plurality of fuse elements for each replacing a defective circuit element therewith is provided on a surface of said semiconductor substrate in such a manner as to be electrically connected with said circuit formation portion, and

wherein at least one seal ring each made of a conductive

layer is formed in such a manner as to surround said plurality of fuse elements, said at least one seal ring being connected with said semiconductor substrate and extending over said plurality of wiring insulating films.

27. The semiconductor device according to claim 26, wherein, at least one bottomed seal ring, being not connected with said semiconductor substrate, is formed in such a manner as to surround said plurality of fuse elements.

28. The semiconductor device according to claim 26, wherein said at least one seal ring comprises a damascene wiring structure.

29. The semiconductor device according to claim 27, wherein said at least one bottomed seal ring comprises a damascene wiring structure.